



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,436	12/12/2001	Timothy B. Cowles	00-0058.02	4282

7590 09/30/2004

Charles Brantley  
Micron Technology, Inc.  
8000 S. Federal Way  
Boise, ID 83716

EXAMINER

TU, CHRISTINE TRINH LE

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/022,436	<b>Applicant(s)</b> COWLES ET AL.	
	<b>Examiner</b> Christine T. Tu	<b>Art Unit</b> 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 July 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) 1-6 and 10-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 10-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 December 2001 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>12/12/01; 4/21/02; 6/12/03</u>  | 6) <input type="checkbox"/> Other: _____                                    |

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (6,246,618 and Yamamoto hereinafter).

Claim 1:

Yamamoto discloses the invention substantially as claimed. Yamamoto teaches (figures 1 and 3) that a LSI comprises plurality of RAMs (10, 11, 12, 13) which are simultaneously tested by a BIST block (2) during BIST mode. The BIST block comprises a code generator (84) for generating a repair code signal comprising a memory specification information signal. The memory specification information signal

Art Unit: 2133

shows which RAM of the RAMs is defective (figures 3 and 1, column 7 line 24-column 8 lines 30).

Yamamoto does not explicitly teach storing of the repair code signal. However, it would have been obvious to one skilled in the art at the time the invention was made to modify such that the repair code signal including memory specification information signal would have been stored. One having ordinary skill in the art would be motivated to realize so because the storing the repair code signal would depends on the necessity of delay for later use of such a repair code signal.

Claims 2-6:

Yamamoto teaches that the RAMs (11-13) are parts of the LSI (10) which can be an electronic system, a computer system, telephone system.

Claims 10-12:

Yamamoto discloses the invention substantially as claimed. Yamamoto teaches (figures 1 and 3) that a LSI comprises plurality of RAMs (10, 11, 12, 13) which are simultaneously tested by a BIST block (2) in responsive to a BIST mode. A test/repair control logic (2) sends control signals (signals for testing which include data and control signals) to the memory inputs of selectors (20-23) (figure1, column 5 lines 34-38 and column 6 lines 64-column 6 line 5).

Yamamoto does not explicitly teach the system has a primary function other than test or repair function. However, Yamamoto teaches that the LSI can be in actual


Art Unit: 2133

operation besides testing operation (column 6 lines 3-5). It would have been obvious to one skilled in the art at the time the invention was made to realize that Yamamoto's actual operation would have been a primary function. The artisan would have been motivated to interpret such that the recited "primary function" does not exclude from the inclusion of Yamamoto's actual (normal) operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (703)305-9689. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Christine T. Tu  
Primary Examiner  
Art Unit 2133

September 25, 2004